WHAT IS CLAIMED IS:

1. A method for treating a semiconductor device comprising passivating said device with deuterium.

2. The method of claim 1 wherein:
said semiconductor device comprises silicon.

3. The method of claim 1 wherein said passivating includes the steps of:
subjecting said device to a heated, deuterium gas-enriched ambient.

4. The method of claim 1 wherein said passivating includes:
implanting atomic or ionic deuterium into said device; and
heating said device.

5. The method of claim 1 wherein said device includes:
a silicon layer; and
an insulative layer adjacent said silicon layer.

6. The method of claim 1 wherein said semiconductor device includes a plurality of active components.

7. The method of claim 3 wherein said deuterium-enriched ambient comprises deuterium gas and one or more inert gases.

8. The method of claim 7 wherein said ambient includes 1% to 100% by volume deuterium gas.

9. The method of claim 5 wherein said ambient comprises deuterium gas and one or more of hydrogen, nitrogen, argon, and helium gas.

10. The method of claim 5 wherein said insulative layer comprises an oxide or nitride of silicon.

11. The method of claim 7 wherein said device also includes:

a conductive layer adjacent said insulative layer.

12. The method of claim 3 which comprises heating said device at a temperature of at least about 200°C.

13. The method of claim 4 which comprises heating said device at a temperature of at least 200°C.

14. The method of claim 12 which comprises heating said device at a temperature of about 200°C to about 1000°C while flowing a deuterium-enriched ambient over said device.

15. A semiconductor device passivated with deuterium.

16. The device of claim 15 which comprises semiconductor containing one or more elements from Group III, Group IV or Group V of the periodic table.

17. The device of claim 15 which comprises a semiconductor consisting essentially of silicon or gallium arsenide.

18. The device of claim 16 which includes:

a semiconductive silicon layer; and

an insulative layer adjacent said semiconductive layer.

19. The device of claim 18 wherein said insulative layer comprises oxide or nitride of silicon.

20. The device of claim 19 which includes a conductive layer adjacent the insulative layer.

21. The device of claim 20 wherein said conductive layer comprises metal, polysilicon, titanium nitride or a metal silicide.

22. The device of claim 21 wherein said conductive layer comprises a metal selected from aluminum, gold, and copper; a metal silicide selected from tungsten, molybdenum, tantalum, titanium, nickel and cobalt silicide, or a combination thereof; polysilicon; or titanium nitride.

23. A semiconductor device, comprising:

a semiconductive layer comprising a Group III, IV or V element, or a mixture thereof;

an insulative layer adjacent said semiconductive layer; and

wherein deuterium atoms are covalently bound to atoms of said Group III, IV or V element so as to increase the resilience of said device to hot carrier effects.

24. The device of claim 23, wherein:

said semiconductive layer is silicon and said insulative layer comprises oxide or nitride of silicon.

25. The device of claim 24 which further comprises:

a conductive layer atop said insulative layer.

26. The device of claim 25, which is a metal oxide semiconductor field effect transistor.

27. The device of claim 25, which includes a plurality of active components.

28. A method for conditioning a semiconductor device to increase its resilience to hot carrier effects, comprising:

disposing atomic, molecular or ionic deuterium in an area of said device subject to hot carrier effects; and

heating said device.

29. The method of claim 28 in which said device includes at least one metal oxide semiconductor field effect transistor.

30. The method of claim 29 in which said device includes a plurality of metal oxide semiconductor field effect transistors.

31. The method of claim 28 in which said device includes:

a crystalline silicon semiconductive layer;

a silicon dioxide layer atop said semiconductive layer; and

a conductive layer atop said silicon dioxide layer.

32. The method of claim 28 in which said device includes a silicon nitride layer, and wherein the method includes trapping the molecular deuterium within layers of the semiconductor device during fabrication.

33. A method of operating a semiconductor device with resistance to hot carrier defects, comprising:

operating a semiconductor device under conditions which create hot carriers which interact with the interface of a semiconductor layer and an insulative layer of the device, said semiconductor having been passivated with deuterium.

34. The method of claim 33 wherein said device includes a plurality of metal oxide semiconductor field effect transistors.

35. The method of claim 34 wherein said device includes:

a crystalline silicon semiconductive layer;

a silicon dioxide layer atop said semiconductive layer; and

a conductive layer atop said silicon dioxide layer

36. An encapsulated semiconductor unit, comprising:

a semiconductor device passivated with deuterium; and

an encapsulation over said semiconductor device.

37. The method of claim 36, wherein said semiconductor device includes a plurality of metal oxide semiconductor field effect transistors.

38. The method of claim 37, wherein said device includes a crystalline silicon semiconductive layer.

39. The method of claim 38, wherein said device includes:

a silicon dioxide layer atop said semiconductive layer; and

a conductive layer atop said silicon dioxide layer.